SEMICONDUCTOR DEVICES WITH SCALABLE TWO TRANSISTOR MEMORY CELLS AND METHODS OF FABRICATING THE SAME

Abstract of the Disclosure

Semiconductor devices having scalable two transistor memory cells, and methods of fabricating the same, are disclosed. The semiconductor devices include a semiconductor substrate having first, second and third isolation layers thereon. The first and second isolation layers are spaced apart to define a first active region therebetween, and the second and third isolation layers are likewise spaced apart to form a second active region therebetween. A cell gate is provided on each active region that includes a gate dielectric layer, a storage node, a multiple tunnel junction barrier and a source layer that are sequentially stacked. The device also includes first and second control lines that surround at least a portion of each sidewall of the cell gates. A dielectric layer may be interposed between the sidewalls of the cell gates and the control line that surrounds it. A data line connects to the cell gates.

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